Appln. No.: 09/942,835
Amendment Dated March 17, 2004
Reply to Office Action of December 17, 2003

Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Currently Amended) A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer ~~and~~

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes configured to define ~~defining~~ at least two charge wells, in the substrate, in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type but having a different dopant concentration than the substrate, in the inter-electrode gap; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

~~means for stabilizing the inter-electrode gap.~~

2. (Canceled)

3. (Currently Amended) A charge coupled device according to claim 1, wherein the apparatus ~~means~~ for stabilizing the inter-electrode gap further includes:

a further dielectric layer formed over the at least two gate electrodes; and

a further gate electrode formed overlying the further dielectric layer and selectively positioned over the inter-electrode gap.

4. - 6. (Canceled)

7. (Currently Amended) A charge coupled device made according to a standard CMOS process on a substrate of a first conductivity type, the charge coupled device comprising:

a dielectric layer overlaying at least a portion of the substrate, the dielectric layer being a CMOS gate dielectric layer; ~~and~~

at least two gate electrodes overlaying the dielectric layer, the at least two gate electrodes defining at least two charge wells, in the substrate, in response to a bias potential applied to the at least two gate electrodes, the at least two gate electrodes being separated by an inter-electrode gap; and

~~a~~ means for stabilizing the inter-electrode gap including means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field[[s]] to extend across the inter-electrode gap from ~~the~~ at least one of the at least two gate electrodes to stabilize the inter-electrode gap.

8. (Original) A charge coupled device according to claim 1, wherein a first one of the charge well areas and its corresponding gate electrode form a photogate optical sensor and the charge coupled device further comprises:

a well region of a first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

9. (Original) A charge coupled device according to claim 8, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

10. (Original) A charge coupled device according to claim 9, wherein the plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

11. (Currently Amended) An optical sensor circuit for receiving photocarriers from a source and being formed on a single monolithic substrate comprising:

a charge coupled device (CCD) array, the array being formed of a plurality of single polysilicon CMOS pixels, each pixel including,

a semiconductor layer of a first conductivity type formed on the substrate;

a first dielectric layer overlaying the semiconductor layer, ~~substrate,~~ the first dielectric layer being a CMOS gate dielectric layer;

at least two gate electrodes overlaying the first dielectric layer and configured to define ~~defining~~ at least two charge wells, respectively, in the semiconductor layer, in response to a bias potential applied to the at least two gate electrodes, wherein adjacent ones of the at least two gate electrodes are separated by an inter-electrode gap, a combination of one of the at least two charge wells and its respective overlaying gate electrode forming a photogate optical sensor and a combination of another one of the at least two charge wells and its respective overlaying gate electrode forming a transfer gate; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type but having a different dopant concentration than the semiconductor layer, in the inter-electrode gap; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

~~means for stabilizing the inter-electrode gap.~~

12. (Canceled)

13. (Original) An optical sensor according to claim 11, further comprising:

a well region of the first conductivity type, adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and

a diffusion region of a second conductivity type, different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

14. (Original) An optical sensor according to claim 13, further including:

a further well region of the first conductivity type, the further well region forming a further charge barrier well; and

a plurality of further diffusion regions of the second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink and a plurality of transistors, wherein one of the at least two gate electrodes that is not a photogate overlies a portion of the further charge barrier well adjacent to the charge sink.

15. (Original) A charge coupled device according to claim 13, wherein the plurality of transistors include a reset transistor and an emitter follower amplifier, both coupled to the charge sink.

16. (Original) An imager system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array.

17. (Original) A camera system comprising:

a single monolithic integrated circuit including:

a charge coupled device (CCD) imager array; and

a complementary metal oxide semiconductor (CMOS) analog to digital converter coupled to receive image signals from the CCD imager array; and

optics configured to focus radiation onto the CCD imager array.

18. (Currently Amended) A charge coupled device made according to a standard single polysilicon CMOS process, the charge coupled device comprising:

a substrate of a first conductivity type;

a well region of a second conductivity type, opposite to the first conductivity type;

an oxide layer formed over at least the well region, the oxide layer being a CMOS gate oxide layer;

first and second polysilicon gate electrodes formed on the oxide layer over the well region, the first and second gate electrodes being separated by an inter-electrode gap, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register; and

apparatus for stabilizing the inter-electrode gap selected from a group consisting of:

a semiconductor region of the first conductivity type but having a different dopant concentration than the substrate, in the inter-electrode gap; and

means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

19. (Canceled)

20. (Original) A back illuminated imager comprising:

a substrate of a first conductivity type having a front side and a back side;

a photodetector formed in the front side of the substrate;

a well region of a second conductivity type, opposite to the first conductivity type, formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction; and

at least one diffusion region in the well region of the second conductivity type forming a component of the back illuminated imager;

whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction.

21. (Previously Presented) An electronic camera system comprising:

an imager formed according to one of claims 18 and 20; and

optics that are configured to focus radiation onto the imager.

22-30 (Cancelled)

31. (Currently Amended) The charge coupled device of claim 11 ~~1~~, wherein the semiconductor layer is ~~the charge coupled device includes~~ a transmission channel and the transmission channel is a CMOS N-well.

32. (Currently Amended) The charge coupled device of claim 1, wherein the at least two gate electrodes include at least two CMOS polysilicon gate electrodes.